**CLAIMS**

1. An apparatus comprising:

a shared memory configured to store data; and

a multiprocessor logic circuit comprising a plurality of processors and a message circuit, wherein said message circuit is a configured to pass messages between said processors.

2. The apparatus according to claim 1, wherein said message circuit comprises a dedicated messaging circuit.

3. The apparatus according to claim 1, wherein said message circuit comprises a message pipe-line FIFO.

4. The apparatus according to claim 1, wherein said message circuit is further configured to provide bi-directional orderly command passing.

5. The apparatus according to claim 1, wherein said message circuit is further configured to generate one or more control signals, said control signals configured to control an operation of said processors.

6. The apparatus according to claim 5, wherein said control signals comprise signals selected from the group consisting of (i) pipe-line overflow signals, (ii) pipe-line available signals, and (iii) command pending signals.

7. The apparatus according to claim 1, wherein said message circuit is further configured to add commands with normal priority levels and urgent priority levels.

8. The apparatus according to claim 7, wherein said normal priority levels comprise adding commands to an end of a message queue and said urgent priority levels comprise adding commands to a near to front of said message queue.

9. The apparatus according to claim 1, wherein said multiprocessor logic circuit further comprises:

an address decoder configured to decode a system address and control said message circuit.

10. The apparatus according to claim 1, wherein said apparatus provides a multiprocessor communication and shared memory architecture.

11. The apparatus according to claim 1, wherein:

said multiprocessor logic circuit and said shared memory are coupled by a system bus;

said multiprocessor logic block further comprises an address decoder configured to control said message circuit; and

said message circuit is configured to generate one or more control signals configured to control said processors.

12. An apparatus comprising:

means for storing data with a shared memory;

means for processing data with a plurality of processors; and

means for passing messages between said processors.

13. A method for multiprocessor communication with a shared memory, comprising the steps of:

(A) storing data with said shared memory;

(B) processing data with a plurality of processors; and

(C) passing messages between said processors.

14. The method according to claim 14, wherein step (C) further comprises:

providing bi-directional orderly command passing.

15. The method according to claim 14, wherein step (C) further comprises:

generating one or more control signals, said control signals configured to control an operation of said processors.

16. The method according to claim 15, wherein said control signals comprise signals selected from the group consisting of: (i) pipe-line overflow signals, (ii) pipe-line available signals, and (iii) command pending signals.

17. The method according to claim 13, wherein step (C) further comprises:

adding commands with normal priority levels; and

adding commands with urgent priority levels.

18. The method according to claim 17, wherein:

said adding commands with normal priority levels further comprises adding commands to an end of a message queue; and

said adding commands with urgent priority levels further comprises adding commands to a near to front of said message queue.

19. The method according to claim 13, wherein step (C) further comprises:

decoding a system address.

20. The method according to claim 19, wherein step (C) further comprises:

controlling said messages in response to said decoded system address.